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(54) SEMICONDUCTOR WAFER AND MANUFACTURING METHOD THEREOF AND ITS USE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide an epitaxial semiconductor wafer.
SOLUTION: In a semiconductor wafer constituted of the front face and rear face and an epitaxial layer made of semiconductor materials deposited on the front face, the epitaxial layer has a maximum local mean value SFQRmax of 0.13 μm or less and the maximum density of 0.14 at the center of scattered lights per 1 cm2, and the front face of the semiconductor wafer has Surface roughness of 0.05-0.29 nmRMS measured by an AFM on a reference face in a size of 1 μm×1 μm before the epitaxial layer is deposited.

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CLAIMS

[Claim(s)]
[Claim 1] The semi-conductor wafer characterized by having the surface roughness of 0.05 which the epitaxial layer measured by AFM in the datum level of 1micrometerx1micrometer magnitude the maximum local flat value SFQRmax of 0.13 micrometers or less, and before it has the maximum consistency based on [0.14] the scattered lights per two 1cm and the front face of a semi-conductor wafer deposited the epitaxial layer - 0.29nmRMS in the semi-conductor wafer which has the epitaxial layer which consists of a semiconductor material which deposited in the front face, the rear face, and the front face.
[Claim 2] In the manufacture approach of a semi-conductor wafer of having the epitaxial layer which consists of a semiconductor material which deposited in the front face, the rear face, and the front face down-stream-processing: (a) of the following [approach / said] -- as only one polish process, supplying an alkaline polish sol The process which grinds the front face and rear face of a semi-conductor wafer to coincidence between the rotating polish disks, A semi-conductor wafer exists in the space of a rotating disk in that case, and the thickness of a rotating disk is adjusted fewer 2-20 micrometers than the thickness of the semi-conductor wafer which carried out finishing polish. (b) Supplying the liquid containing at least one sort of polyhydric alcohol which has 2-6 carbon atoms The process which processes the front face and rear face of a semi-conductor wafer to coincidence between the rotating polish disks, (c) The manufacture approach of the semi-conductor wafer characterized by defecating a semi-conductor wafer and consisting of a process to dry and a process which deposits an epitaxial layer in the front face of the semi-conductor wafer manufactured by (d) process (a) - (c).
[Claim 3] The approach according to claim 2 a semi-conductor wafer and epitaxial covering consist of silicon.
[Claim 4] The approach according to claim 2 or 3 which the alkaline polish sol used at a process (a) consists of suspension of an underwater silicon dioxide particle and inorganic, and/or an organic base substantially, and this suspension has pH values 9-12, and is supplied continuously.
[Claim 5] An approach given [to claims 2-4 containing at least one sort of polyhydric alcohol chosen from the group of the compound with which the liquid used at a process (b) consists of ethylene glycol, a glycerol, propylene glycol, and a butylene glycol] in any 1 term.
[Claim 6] The approach containing at least one sort of matter chosen from the group of the compound with which the liquid used at a process (b) consists of monohydric alcohol and a surfactant according to claim 5.
[Claim 7] The method given [to claims 2-6] in any 1 term of having the thickness whose epitaxial layer which deposits at a process (d) is 0.3-10 micrometers, and depositing at the temperature of 900-1250 degrees C.
[Claim 8] An approach given [to claims 2-7 which carry out hydrophilization of the epitaxial layer which deposits at a process (d) using oxidation gas] in any 1 term.
[Claim 9] An approach given [to claims 2-7 which carry out hydrophilization of the epitaxial layer which deposits at a process (d) to a wet chemistry target] in any 1 term.
[Claim 10] An approach given [to claims 2-9 which manufacture a semi-conductor wafer, process with a grinding operation before polish, and carry out grinding of one side or both sides of a semi-conductor wafer by cutting a semiconducting crystal in that case] in any 1 term.
[Claim 11] The approach according to claim 10 of making the edge of a semi-conductor wafer round in front of the grinding of a semi-conductor wafer, or in the back.

[Claim 12] An approach give[redacted]o claims 2-11 which carry out an etching [redacted]ess before polish of a semi-conductor wafer, and remove an ingredient from each of two wafer sides] in any 1 term.
[Claim 13] Use for manufacturing the semi-conductor structural part with which the semi-conductor wafer which is manufactured by the approach given [to claims 2-12] in any 1 term, and which was made epitaxial was accumulated.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the semi-conductor wafer which has a number based on [where it decreased on the improved display flatness and an epitaxial layer] light scattering and which has epitaxial covering in a front face, and its cheap manufacture approach.
[0002]
[Description of the Prior Art] This kind of semi-conductor wafer is suitable in order to manufacture the electronic structure components especially whose line breadth is 0.13 micrometers or less in order to use it for semi-conductor industry.
[0003] The semi-conductor wafer which is suitable in order to manufacture the electronic structure components especially whose line breadth is 0.13 micrometers or less must have many special properties. Especially an important property is the local display flatness of a semi-conductor wafer. A modernistic stepper technique needs the optimal local display flatness in all the subregions of one field of a semi-conductor wafer expressed as SFQR (the least squares/range made into criteria in the front face of a site front-surface referenced least squares/ranges site = the range of a variation rate forward [from the front face determined by minimization of the error square for the structural part side of the decided dimension], and negative). A SFQRmax value shows the maximum SFQR value about all the structural part sides on a semi-conductor wafer. Under the regulation generally accepted, it is mentioned that must be equal to the line breadth of the semi-conductor structural part which should be manufactured to this possible on this wafer, or the SFQRmax value of a semi-conductor wafer must be smaller than this. If it exceeds this value, damage on the structural part concerned will be produced with the problem of a stepper's focus, and it. Other important properties of a semi-conductor wafer are the numbers based on [in the front face by which a semi-conductor structural part is manufactured] light scattering (localized light scatterers LLS local light-scattering object). LLS may produce damage on a structural part in a specific number and a specific value. Generally the final display flatness of a semi-conductor wafer is obtained according to a polish process. In order to improve the display flatness of a semi-conductor wafer, the equipment and the approach of grinding the front face and rear face of a semi-conductor wafer to coincidence were prepared, and it was developed further. This so-called double-sided grinder is indicated by for example, the U.S. Pat. No. 3691694 specification. A polish sol is made to exist between two rotating polish disks which stuck abrasive cloth in the rotating disk which consists of the metal or the plastics which has the space which adjusted the semi-conductor wafer in the suitable dimension by the configuration of the double-sided grinder indicated by the Europe patent No. 208315 specification , it is made to exercise on the path beforehand decided with the machine parameter and the processing parameter , and this grinds . By English reference, this rotating disk is called a "carrier." In the German patent specification of the application number 19905737.No. 0, the double-sided grinding method which produces the semi-conductor wafer which has the display flatness improved by part especially for a edge is indicated. The rotating disk with which thickness is adjusted so that the last thickness of the wafer by which finishing polish was carried out at that time may become larger 2-20 micrometers than the thickness of a rotating disk is used.
[0004] The silicon wafer which has, the semi-conductor wafer, for example, the silicon layer, of the single crystal which has the so-called epitaxial layer or so-called epitaxial growth phase with which the growth phase of the same single crystal of crystal orientation and a semi-conductor structural part are covered, is

compared with the semi-conductor wafer which consists of a uniform ingredient, and has the advantage of shoes. The so-called problem of a latch rise is mentioned to the 1st in this case, this may be generated into a uniform ingredient for example, in a bipolar CMOS circuit, an electrical potential difference may be produced in a bipolar transistor, and this may enable the inversion of a charge and may produce the short circuit of the structural part concerned. It is common knowledge that the problem of this latch rise can be effectively prevented by use of the semi-conductor wafer which consists of a substrate wafer (low electric resistance) of high doping and an epitaxial layer (high resistance) of low doping and which was made epitaxial at this contractor, and this produces the getter effectiveness of a request of a substrate in coincidence, and decreases consumption of the flat surface of a structural part further. Furthermore, the front face made epitaxial has low defect density as compared with the polished semi-conductor wafer which may be the so-called COPs (crystal-originated particles crystal origin particle), for example and which is expressed as LLS, and, generally this produces the higher yield of an unhurt semi-conductor structural part. Furthermore, an epitaxial layer does not have the oxygen content which should be mentioned especially, but the risk of the oxygen precipitate which destroys by this the circuit in the range relevant to a structural part which may happen is eliminated.

[0005] The surface roughness after the cutting polish which manufactured the semi-conductor wafer made epitaxial by the process sequence of cutting polish-finishing polish-defecation-epitaxy from the suitable reserve product, and was measured by the technical level using the atomic force microscope method (AFM) in 1micrometerx1micrometer at that time is about 0.5 to 3 nmRMS (square mean square root granularity) according to a practice, and is about 0.05 to 0.2 nmRMS after finishing polish. Three steps or four steps of polish processes are well-known similarly, and granularity decreases gradually in this case. Before processing a semi-conductor wafer at a finishing polish process on the Europe patent public presentation No. 684634 specifications, the strange method which carries out sequential supply of the two different polish sols of grain size which is different at a cutting polish process is indicated. The fault of the method of grinding a multistage story is that the manufacture costs of a semi-conductor wafer become high with each additional process.

[0006] In order to carry out cutting polish of the silicon wafer which carried out cutting-wrapping-etching processing at the Europe patent public presentation No. 711854 specification, to adjust to the surface roughness of 0.3 - 1.2nmRMS (AFM 1micrometerx1micrometer) in that case and to fall costs, the method of manufacturing the wafer made epitaxial is indicated by by depositing an epitaxial silicon layer, without carrying out the finishing polish process made smooth. In this way, the epitaxial layer manufactured produces the increment in damage on the structural part with which the increment based on [on the epitaxial front face caused by quite high start granularity] light scattering is manufactured on this wafer, although an electrical property is equal to the epitaxial layer generally beforehand manufactured using a finishing polish process.

[0007]

[Problem(s) to be Solved by the Invention] Therefore, especially the technical problem of this invention is offering the semi-conductor wafer which is suitable in order to manufacture the electronic structure components whose line breadth's is 0.13 micrometers or less, does not have the aforementioned fault about the number based on [on an epitaxial front face] light scattering, but is attained by the cheap manufacture approach and which was made epitaxial. Furthermore, the forge fire same at least as the property of the semi-conductor wafer which is manufactured by the technical level and which was made epitaxial of other properties of the semi-conductor wafer made epitaxial must be good.

[0008]

[Means for Solving the Problem] The object of this invention is a semi-conductor wafer which has the epitaxial layer which consists of a semiconductor material which deposited in the front face, the rear face, and the front face. This wafer 0.13-micrometer less or equal reaches maximum local flat value SFQRmax, and an epitaxial layer has the maximum consistency based on [0.14] the scattered lights per two 1cm. Before the front face of a semi-conductor wafer deposits an epitaxial layer, it is characterized by having the surface roughness of 0.05 measured by AFM in the datum level of 1micrometerx1micrometer magnitude - 0.29nmRMS.

[0009] the manufacture approach of a semi-conductor wafer that the object of this invention has further the epitaxial layer which consists of a semiconductor material which deposited in the front face, the rear face, and the front face -- it is -- following down-stream-processing: (a) -- as only one polish process The process which grinds the front face and rear face of a semi-conductor wafer to coincidence between the rotating

polish disks while supplying [redacted]alkaline polish sol, A semi-conductor waf[redacted]ists in the space of a rotating disk in that case, and the thickness of a rotating disk is adjusted fewer 2-20 micrometers than the thickness of the semi-conductor wafer which carried out finishing polish. (b) Supplying the liquid containing at least one sort of polyhydric alcohol which has 2-6 carbon atoms It is characterized by defecating the process and (c) semi-conductor wafer which process the front face and rear face of a semi-conductor wafer to coincidence between the rotating polish disks, and consisting of a process to dry and a process which deposits an epitaxial layer in the front face of the semi-conductor wafer manufactured by (d) process (a) - (c).

[0010] The important description of this invention is that the semi-conductor wafer which is performed by supplying the aquosity liquid containing at least one sort of polyhydric alcohol which has 2-6 carbon atoms and which has high display flatness and low granularity only at one polish process by coincidence polish of the front face of a semi-conductor wafer and a rear face is manufactured. The approach of this invention cannot make the finishing polish process of costs starting and deteriorating the configuration (Geometrie) of a semi-conductor wafer carry out, and produces the semi-conductor wafer which has a front face with very few defects and by which epitaxial covering was carried out.

[0011] The start product of the approach of this invention is the semi-conductor wafer by which it was cut, for example, dissociated from the single crystal which consists of silicon by which grinding was carried out circularly, and the front face and/or the rear face were processed from the crystal using the surface grinding operation by the well-known approach. In the case that this is desirable, in order that a crystal may make a crystallographic axis the same, you may have one or more orientation properties, for example, a notch, and/or flats. The edge of a semi-conductor wafer can be similarly made round in the suitable location of a consecutive-processing process using the grinding plate of a suitable complicated cross-section configuration. Furthermore, possibility of etching the front face of a semi-conductor wafer after a grinding operation exists.

[0012] The end product of the approach of this invention is a semi-conductor wafer which satisfies the demand of the semi-conductor wafer made epitaxial as starting material of the semi-conductor structural part manufacture whose line breadth is 0.13 micrometers or less, and is superior to the semi-conductor wafer manufactured by the technical level based on the abbreviation of high yield and a finishing polish process about the manufacture costs and which was made epitaxial by the front face at least.

[0013] The approach of this invention is processed in principle using the chemical mechanical double-sided grinding method used, and is applicable to manufacture of the disc-like Plastic solid formed from the ingredient which can be made epitaxial. For example, the silicon of the form of the crystalline array (100) crystallized by the Czochrlski method or the band Czochralski method or (110) (111) the single crystal which it has is advantageous. the [of the element periodic table where silicon contains the doping material of some amount in that case, and doping material produces the ingredient of p mold in this case] -- the [which produces the 3 main group's element, for example, boron, and the ingredient of n mold] -- it is distinguished by the 5 main group's element, for example, phosphorus, arsenic, or antimony. Silicon or silicon / germanium is advantageous as an ingredient of epitaxial covering. For example, generally as for epitaxial covering which consists of silicon, unlike the electrical property of a semi-conductor wafer, an electrical property is used for manufacture of the semi-conductor structural part with which this was accumulated with the doping material content. However, this is not necessarily required. Furthermore, it is desirable to grow up without an epitaxial layer containing one of doping material about the use by which the semi-conductor wafer with which this invention was made epitaxial was planned, and this is possible satisfactory similarly. Especially the silicon wafer that has epitaxial covering which consists of silicon is advantageous within the limits of this invention, in that case, both a silicon wafer and an epitaxial layer are p molds, or both are n molds.

[0014] The approach of this invention is suitable especially in order to manufacture the silicon wafer which has the thickness of 400 micrometers - 1200 micrometers especially advantageous from the diameter of 200mm, 300mm, 400mm, and 450mm, and 100 micrometers to several cm. The semi-conductor wafer made epitaxial is applicable to manufacture of a direct semi-conductor structural part as starting material, or can be supplied to the decided purpose after other processings of the rear face by the grinding by the technical level after covering a rear-face seal object, etching, polish, etc., respectively. With manufacture of the wafer which consists of a uniform ingredient, this invention is applicable to manufacture of the semi-conductor substrate formed in a multilayer like a SOI wafer (silicon on a silicon on insulator insulator), and the so-called BONDEDDO wafer (bonded wafers), of course, in spite of losing the advantage of costs in this case.

[0015] The example of manufacture of the silicon wafer which has epitaxial covering of silicon in a front face

explains the approach of this invention further.
[0016] For example, it is possible to process the silicon wafer cut by the internal terebration or the wire saw method by the approach of direct this invention in principle. However, it is worthy to make round a sharp interface, therefore the edge of a mechanical very delicate wafer using the grinding plate of a suitable complicated cross-section configuration, therefore it is advantageous. Furthermore, in order to improve a configuration and to remove the destroyed crystal layer partially, it is possible to process a silicon wafer at wrapping or a mechanical cutting process like grinding, and to decrease removal of the ingredient in a polish process. It is advantageous to process a silicon wafer with a surface grinding operation, and grinding of one side is carried out in that case, or grinding of sequential or both sides is carried out for both sides to coincidence. In order to remove damage on the wafer front face inevitably produced at a mechanical process process, and a wafer edge, and in order to remove the impurity which exists by the case, an etching process can be performed in this location. This etching process can be carried out as plasma treatment as a wet chemical treatment of the silicon wafer in alkaline or acid etching mixture. The acid etching process in the mixture which becomes the German patent specification of the application number 19833257.No. 2 from the condensed aquosity nitric acid and the condensed aquosity hydrofluoric acid by the example of a publication is advantageous.
[0017] Especially the advantageous starting material of down stream processing of this invention is a semi-conductor wafer by it being manufactured by cutting of a silicon single crystal, making the edge of both wafer sides round, carrying out surface grinding succeedingly, removing silicon 10micrometer-100micrometer per field, carrying out wet chemical etching in acid etching mixture, and removing silicon 5micrometer-50micrometer per wafer side which consists of silicon which has the diameter of 200mm or more.
[0018] Down stream processing of this invention (a)
The grinding method for being suitable for manufacture of the semi-conductor wafer with which this invention was made epitaxial is indicated by the German patent specification of the application number 19905737.No. 0. The double-sided grinder of marketing of magnitude suitable in order to carry out, for example, Peter, The machine of the format AC 2000 of Wolters can be used. This grinder consists of the polish disk and the free, horizontally pivotable upper polish disk of a free, horizontally pivotable lower part substantially, and double-sided cutting polish of a silicon wafer is possible for these two disks in a semi-conductor wafer and this case respectively by being covered with abrasive cloth and supplying the alkaline polish sol of suitable chemical composition continuously. Generally many silicon wafers are ground from the reason of costs to coincidence. With the rotating disk which has the space adjusted by sufficient dimension in order to hold a silicon wafer in that case, a silicon wafer is held during polish on the path of the configuration decided with the machine and the parameter of an approach. A rotating disk has an occlusion part, and contacts a grinder through the ring of the rotating inside pin or the ring of a gear and the ring of the outside pin which generally rotates to hard flow, or the ring of a gear, and this is rotating it among both polish disks. Especially, four pieces to six rotating disks are advantageously used for coincidence, and these are covered with at least three silicon wafers arranged at the same spacing at the circular path, respectively.
[0019] The rotating disk may be manufactured in principle from the metal which covered a metal, plastics, the plastics with which fiber was reinforced, or plastics. The rotating disk which consists of plastics with which fiber was reinforced from steel is advantageous. Especially the rotating disk that consists of stainless steel chrome steel is advantageous.
[0020] A rotating disk has one or more space advantageously circular in order to hold one or more silicon wafers. In order to guarantee free movement of the silicon wafer in the rotating rotating disk, the diameter of space must be slightly larger than the silicon wafer which should be ground. In order to prevent damage on the wafer edge under polish with the edge inside the space in a rotating disk, it is important to cover the inside of space with covering which consists of the plastic lining, for example, the polyamide, the polyethylene, the polypropylene, or poly vinylidene JIFURUORIDO of the same thickness as a rotating disk. The thickness of a rotating disk should be adjusted so that the last thickness of the polished wafer may become advantageously larger 2-20 micrometers than the thickness of a rotating disk. 5-100 micrometers of silicon cutting by the polish process are 10-50 micrometers advantageously.
[0021] It carries out by the format and approach which were advantageously learned for within the limits of the embodiment performed about the ratio of thickness by this contractor in the polish process. It grinds using the polyurethane abrasive cloth with which the degree of hardness (Shore A degree of hardness) of 40-120 is

marketed advantageously. Especially the polyurethane cloth that blended the polyethylene fiber of the degree-of-hardness range 60-90 (Shore A degree of hardness) is advantageous. underwater SiO2 which adds an inorganic base, for example, a sodium hydroxide, and a potassium hydroxide, an alkali-metal salt, for example, potassium carbonate, and/or an organic base, for example, tetramethyl ammonium hydroxide, in polish of a silicon wafer -- advantageous -- one to 10 mass % -- it consists of one to 5 mass % especially advantageous, and continuous supply of 9-12, and the polish sol that has the pH value of 10-11 advantageously especially is advantageously desirable. 0.05-0.5 bars of polishing pressures are 0.1-0.3 bars especially advantageous advantageously.

[0022] Down stream processing of this invention (b)

A chemical very reactant hydrophobic wafer front face must be inactivated after termination of a polish process (a). In the range of this invention, this contains at least one sort of polyhydric alcohol which has 2-6 carbon atoms, and is attained by supplying the aquosity liquid which acts as a stop agent. Other aforementioned abrasives are supplied instead of supply of a liquid, and a grinder cannot be opened wide, but simultaneous processing of the front face of the semi-conductor wafer using this stop agent and a rear face is performed between the polish disks which rotate by this, and a reactant wafer front face is not exposed to air oxygen at the meantime. It is indicated that this is important in order to decrease frictional force, and a pressure decreases to 0.02-0.10 bars in that case, therefore this is advantageous. Although supply of the short time of water is possible between supplies of abrasives and a stop agent, the advantage which should be mentioned especially is not produced.

[0023] It is obtained in purity sufficient for manufacture of a semi-conductor wafer as polyhydric alcohol which has 2-6 carbon atoms, and water and the matter of mixable marketing correspond. The ethylene glycol (ethanediol - 1 two), the propylene glycol (propanediol - 1, 2, and -1.3), butylene glycol (1 butanediol - 1, 3, and - 4), and glycerol (propane triol - 1, 2, 3) of concentration of 0.1 - 10 capacity % are used advantageously. Especially the propylene glycol and the glycerol of concentration of 0.3 - 3 capacity % are advantageous. A stop agent can contain short chain monohydric alcohol like the isopropanol of the concentration of further 0.1 - 2 capacity %, and n-butanol. In addition, little addition of oligo alcohol and polymer alcohol, for example, high-class ethylene glycol, polyvinyl alcohol or polyether polyol, and a surfactant is possible. Addition of a strong acidic component or a strong, alkaline component is not desirable. It is because in the case of the 1st the silicon dioxide particle which produces the wafer front face which has a scratch by fluctuation of the pH value which is not controlled may be formed, and the dirt of etching will be produced on a wafer front face when it is the latter.

[0024] Down stream processing of this invention (c)

A silicon wafer is picked out from a grinder after a stop process (b), and it defecates by the technical level and dries. Defecation can defecate many wafers to coincidence in a bath as a batch method, or can be carried out as independent wafer processing, using an atomizing process. Bath washing which is the sequence of for example, aquosity hydrofluoric-acid-pure-water-tetramethyl ammonium hydroxide (TMAH) / hydrogen-peroxide (H2O2)-pure water, and washes all the wafers from a polish process to coincidence in the range of this invention is advantageous, and in order to improve removal of a particle in that case, assistance of the supersonic wave under TMAH/H2O2 bath is advantageous. The equipment operated by for example, the centrifugal desiccation principle, the hot water principle, the MARANGONI principle, or HF / ozone principle for desiccation without dirt is marketed, and it is uniformly advantageous altogether. In this way, the wafer which is obtained and by which double-sided polish was carried out is dried, and it becomes dirty, and it is a hydrophilic property and has [there is no defect accepted with a scratch and the beam of light converged further, and] the granularity of 0.05 - 0.29nmRMS by AFM measurement (1micrometerx1micrometer) according to the selected polish conditions and the selected polish means. for example, a commercial capacity type -- or measurement with the configuration measuring device (Geometriemessgeraet) operated optically shows the local configuration value SFQRmax of 0.13 micrometers or less about a 25mmx25mm structural part flat surface.

[0025] Down stream processing of this invention (d)

Process (a) The silicon wafer processed by - (c) is equipped with an epitaxial silicon layer in a front face at least by the standard approach. Advantageously, with a CVD method (chemical vapor deposition chemical vapor deposition), silanes, for example, a silane, SiH4, dichlorosilane, SiH2Cl2 or trichlorosilane, and SiHCl3 are supplied to a wafer front face, it decomposes into the silicon and the volatile by-product of an element at

the temperature of 900-1250 degrees C here, and this is performed by forming the silicon layer which epitaxial one, i.e., a single crystal, carries out orientation to a semi-conductor wafer crystallographically, and grows. Si isotope mixture which exists naturally advantageously in that case is used. However, it is possible similarly to use Si isotope mixture artificial in the range which deteriorated or Si pure isotope of this invention. A silicon layer grows epitaxially by the thickness of 0.3-10 micrometers advantageously. The epitaxial layer may be intentionally doped with boron, phosphorus, arsenic, or antimony, in order not to be doped or to adjust to the class of electric conduction, and desired conductivity.

[0026] The semi-conductor wafer of this invention which can be supplied to the processing followed for manufacturing the structural part which has a hydrophobic front face in it and was accumulated on it in this form at least after [the semi-conductor wafer which consists of silicon advantageously especially] performing epitaxial covering of silicon in a front face advantageously especially exists. However, though it is not necessarily required in the range of this invention, in order to protect from contamination, it is possible to carry out hydrophilization of the silicon front face, namely, to cover it with the oxide layer with a thickness of about 1nm known by the thin oxide layer, for example, this contractor, as a natural oxidation object. This can be performed in two different formats in principle. One can be processed by the gas which carries out the oxidation of the front face of the semi-conductor wafer made epitaxial, for example, ozone, and this may be performed within the equipment which is the inside of epitaxial space itself, or was separated. The hydrophilization in the bath equipment accompanied by the continuous bath of the RCA type which follows desiccation of a wafer on the other hand is possible.

[0027] The semi-conductor wafer which has the front face which does not have the cover made epitaxial by the front face at least after operation in down-stream-processing [of this invention] (a) - (d) exists, and before processing this in order to manufacture a semi-conductor structural part, it can be supplied to property-ization of the property. for example, a commercial capacity type -- or measurement with the configuration measuring device operated optically shows the local configuration value SFQRmax of 0.13 micrometers or less about a 25mmx25mm structural part side. The measurement using the optical surface-analysis equipment operated with the laser base shows the maximum consistency based on [0.14] the scattered lights per two 1cm of wafer front faces made epitaxial.

[0028] When required, in for example, laser record, in the edge polish before grinding or to the back, the laser record for a wafer check in the suitable location of a continuous process and/or an edge polish process can be inserted in before double-sided polish, between, or the back. For example, a series of down stream processing of an and also [it is the need] is incorporable into predetermined manufacture like spreading of rear-face covering which consists of polish recon, a silicon dioxide, and/or silicon nitride by the approach similarly learned by this contractor in the suitable location of a continuous process. Furthermore, it is advantageous to process a semi-conductor wafer before each down stream processing or to the back by batch type wafer washing or each wafer washing by the technical level.

[0029] For example, the semi-conductor wafer which is manufactured by this invention and which was made epitaxial does not have a fault compared with the semi-conductor wafer which manufactured the epitaxial layer by the technical level using the finishing polish process before depositing and which was made epitaxial about the parameter known by this contractor used for the metal contamination on the front face of a wafer, the durable time amount of a a small number of charge carrier, and property-ization of other common wafers like a nano topology property.

[0030] As for the semi-conductor wafer which is manufactured by this invention and which was made epitaxial, especially the silicon wafer which has epitaxial silicon covering, line breadth fills the demand of manufacture of a semi-conductor structural part 0.13 micrometers or less. It is indicated that the approach of this invention is the optimal solution for manufacturing the silicon wafer which has the aforementioned description and which was made epitaxial. A demand of the configuration (Geometrie) imposed on starting material is min, and this decreases a demand of a last process. The process which the costs for being connected with the risk of the destruction which decreased after removal of already quite few ingredients and with high processing safety, and being generated with very high yield, for example, correcting the local configuration (localen Geometrie) by plasma etching require is not required for the good configuration attained at the process of this invention, and when there is no need for operation of a finishing polish process, it is completely maintained by the end product of this invention. It was unexpected it not only to excel the semi-conductor wafer with which consecutive processing of this invention is manufactured by the technical

level in the property, but to have had an important advantage compared with the wafer of a technical level about manufacture costs by skipping a finishing polish process to coincidence, and it was not predicted.
[0031]
[Example] All of an example and the example of a comparison given in the following are related with manufacture of the silicon wafer which has the epitaxial silicon layer which produces resistance of the silicon wafer which has the diameter (300**0.2) mm, the oxygen content (6**1) x1017 atom / cm3, and boron doping which produce resistance of the range of 5-20m ohm/cm, and the range of 1-10ohms/cm, and which has boron doping in a front face. For this reason, the required single crystal was extended by the technical level, and it cut short, and the edge was made round and it cut to the wafer which has the thickness cut by the end product by the commercial wire saw. After making an edge round, the rotation grinding machine performed the surface grinding operation with the diamond of the grain size of 600 meshes, and silicon 30micrometer was cut from the front face of a wafer, and the wafer side, respectively at that time. The acid etching process was carried out by the flow etching method following this, and coincidence cutting of the 10 micrometers of each silicon per wafer side was carried out by being immersed in the mixture which consists of nitric-acid 90 mass % (70 in aquosity solution mass %) which condensed the rotating disk, condensed hydrofluoric-acid 10 mass % (50 in aquosity solution mass %), and lauryl ammonium-sulfate 0.1 mass % in that case. Temperature control of the etching mixture was carried out to (20**1 degree C), and nitrogen gas was flowed through.
[0032] Example 1 -- in this example, 300mm silicon wafer which has etched 815 micrometers in a front face and thickness was used. Furthermore, these have the space with a bore of 301mm which covered the polyamide arranged at intervals of [circular / same] three pieces in the circular slot, respectively by using five rotating disks which consist of stainless steel chrome steel which has 770 micrometers in a front face and thickness which were wrapped, and it is Peter about 15 300mm silicon wafers. It made it possible to carry out coincidence polish with the double-sided grinder of the format AC 2000 of Wolters.
[0033] Process (a): Polyurethane abrasive cloth reinforced with the polyethylene fiber of marketing on which the double-sided polish process was stuck by the polish disk of the upper part and a lower part, respectively, and which has a degree of hardness 74 (Shore A) Format Levasil of Bayer which has the pH value adjusted by 10.5 by addition of SiO2 solid-state content 3 mass %, potassium carbonate, and a calcium hydroxide using SUBA500 of Rodel It carried out by 0.15 bar of press ** using the polish sol of 200. It ground at the upper part polish disk temperature of 40 degrees C, and lower part polish disk temperature, respectively, and the cutting speed of 0.60 micrometers/m was produced.
[0034] (Process b): End supply of abrasives after attaining the thickness of the 775micrometer polished wafer, and it is the time amount for 3 minutes, Took the place of the supply of a stop agent which consists of an aquosity solution of glycerol 1 capacity %, n-butanol 1 capacity %, and surfactant 0.07 capacity % of marketing of a trade name Silapur (alkylbenzene sulfonic acid and constituent manufacturer on the basis of an amine ethoxy rate ICB), a polish disk, a downward upper polish disk, and a downward rotating disk were made to exercise further in that case, and the pressure was decreased to 0.05 bars.
[0035] Process (c): The polished silicon wafer was picked out from the grinder, and it washed in the batch type washing station in order of the bath of aquosity hydrofluoric-acid-pure-water-TMAH/H2O2-/supersonic-wave-pure water, and dried in the dryer of marketing operated by the MARANGONI principle with isopropanol. This wafer had surface roughness 0.24nmRSM (AFM 1micrometerx1micrometer).
[0036] Process (d): It is Applied to the silicon wafer which carried out /desiccation and which carried out washing, and was ground. Format Centura of Materials The front face was equipped with the epitaxial growth silicon layer in the epitaxial reactor of HT308, SiHCl3 was used as a silicon component at that time, and resistance was adjusted by doping of diboron hexahydride and B-2 H6. The layer with a thickness of 2.8 micrometers was deposited at the reaction space temperature of 1090 degrees C, and the deposit rate of 3 micrometers/m.
[0037] With the property-ized silicon of the silicon wafer made epitaxial, hydrophilization of the silicon wafer made epitaxial was carried out by the technical level in bath equipment to the front face, and it dried in it, and property-ized about the defect of the front face made epitaxial with the surface-analysis equipment operated by the laser principle of the format SP 1 of KLA-Tencor. Under [the average 51**20 is acquired all over a DWN (dark field wide) slot about the total of a LLS defect 0.12 micrometers or more and equivalent to LLS/cm (0.07**0.03)3]. The wafer was succeedingly measured about the local configuration with the

configuration measuring devi[redacted]operated by the capacity principle of the fo[redacted]t AFS of the ADE shrine which has 3mm of edge exclusion. Average (0.10**0.01) mum was obtained about the SFQRmax value (mesh 25mmx25mm).

[0038] Levasil200 [underwater instead of the liquid of the above / inside / of a stop process / on the basis of a glycerol] although carried out like [1] the publication one example of a comparison The mixture which consists of 3 mass % and n-butanol 1 capacity % was used. The polished wafer had granularity 0.55nmRMS after washing and desiccation (AFM1micrometerx1micrometer). after epitaxial covering and hydrophilization and a front face -- the average of a LLS defect a DWN slot -- considerable and SFQRmax average (0.10**0.01) mum were determined as 0.12mm or more and LLS/cm (0.52**0.18)2 368**124 inside.

[0039] Although carried out like the publication for the example 1 of example of comparison 2 comparison, before carrying out epitaxial covering, the finishing polish process of the front face of a wafer by the technical level was inserted. Format Glanzox3900 of having soft polyurethane abrasive cloth, SiO2 solid-state content 2 mass %, and a pH value 10 in that case The aqueous suspension of the abrasives of FUJIMI was used. The wafer was washed by the RCA method after removing silicon 0.5micrometer by 0.15-bar press **, and it dried using the MARANGONI dryer. The granularity of the front face which carried out finishing polish was 0.09nmRMS(s) (AFM1micrometerx1micrometer). The measured value below after [in the front face which carried out finishing polish] an epitaxial silicon deposit was obtained. the average of the front number of LLS defects the inside of DWN slot 78 **23 -- 0.12 micrometers or more and LLS/cm (0.11**0.03)2 -- considerable and SFQRmax average (0.12**0.03) mum.

[0040] The front face, rear face, and edge of 300mm silicon wafer manufactured by other examples of the property-ized above of a wafer and two examples of a comparison which were manufactured were property-ized about the metal contamination, the a small number of charge carrier durable time amount, and the nano topology property on the front face of a wafer by the well-known approach to this usual contractor. A material difference was not statistically accepted between each trial groups.

[Translation done.]